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[MULTI-GATE DRAM WITH DEEP-TRENCH CAPACITOR AND FABRICATION THEREOF]

Abstract

A multi-gate DRAM cell is described, including a multi-gate transistor and a deep trench capacitor. The transistor includes a semiconductor pillar, a multi-gate, a gate dielectric layer, a first and a second source/drain regions. The pillar is beside the deep trench capacitor not overlapping with the latter. The multi-gate is at least on three sidewalls of the pillar separated by the gate dielectric layer, and can be a treble gate or a surrounding gate. The first source/drain region is in the top portion of the pillar, and the second source/drain region in the pillar coupling with the deep trench capacitor.